What is claimed is:

1. A signal detection circuit, comprising:

first and second power supply terminals;

first and second input terminals;

a first output terminal;

a first resistor coupled between the first input terminal and a first level-shifted input signal node;

a first transistor having a drain coupled to the first level-shifted input signal node, a gate coupled to a common node, and a source coupled to the first power supply terminal;

a second resistor coupled between the second input terminal and a second level-shifted input signal node;

a second transistor having a drain coupled to the second level-shifted input signal node, a gate coupled to the common node, and a source coupled to the first power supply terminal;

a third resistor coupled between the first input terminal and the common node;

a fourth resistor coupled between the second input terminal and the common node;

a third transistor having a gate and a drain coupled to the common node and a source coupled to the first power supply terminal;

a first voltage source coupled between the common node and a first threshold node;

a second voltage source coupled between the common node and a second threshold node; and

a first comparator comprising:

a fourth transistor having a drain coupled to a first node, a gate coupled to the first threshold node, and a source coupled to the first power supply terminal;

a fifth transistor having a drain coupled to the first node, a gate coupled to the second threshold node, and a source coupled to the first power supply terminal;

a sixth transistor having a gate and a drain coupled to the first node, and a source coupled to the second power supply terminal;

a seventh transistor having a drain coupled to the first output terminal, a gate coupled to the first node, and a source coupled to the second power supply terminal;

an eighth transistor having a drain coupled to the first output terminal, a gate coupled to the first level-shifted input signal node, and a source coupled to the first power supply terminal; and

a ninth transistor having a drain coupled to the first output terminal, a gate coupled to the second level-shifted input signal node, and a source coupled to the first power supply terminal.

2. The signal detection circuit of claim **1**, further comprising:

a first capacitor coupled between the first input terminal and the first level-shifted input signal node; and

a second capacitor coupled between the second input terminal and the second level-shifted input signal node.

3. The signal detection circuit of claim **2**, wherein:

the first voltage source comprises a first programmable current source coupled to the first threshold node, and a fifth resistor coupled between the common node and the first threshold node; and

the second voltage source comprises a second programmable current source coupled to the second threshold node, and a sixth resistor coupled between the common node and the second threshold node.

4. The signal detection circuit of claim **3**, wherein the first and second programmable current sources comprise:

a differential to single-ended amplifier having an inverting input terminal coupled to a reference voltage terminal, a non-inverting input terminal coupled to a feedback node, and an output terminal coupled to a bias node;

a tenth transistor having a drain coupled to the feedback node, a gate coupled to the bias node, and a source coupled to the first power supply terminal;

a seventh resistor coupled between the feedback node and the second power supply terminal;

a first dual-gate transistor having a drain coupled to a second node, a first gate coupled to the bias node, a second gate coupled to a first logic terminal, and a source coupled to the first power supply terminal;

a second dual-gate transistor having a drain coupled to the second node, a first gate coupled to the bias node, a second gate coupled to a second logic terminal, and a source coupled to the first power supply terminal;

a third dual-gate transistor having a drain coupled to the second node, a first gate coupled to the bias node, a second gate coupled to a third logic terminal, and a source coupled to the first power supply terminal;

a fourth dual-gate transistor having a drain coupled to the second node, a first gate coupled to the bias node, a second gate coupled to a fourth logic terminal, and a source coupled to the first power supply terminal;

an eleventh transistor having a gate and a drain coupled to the second node, and a source coupled to the second power supply terminal;

a twelfth transistor having a drain, a gate coupled to the second node, and a source coupled to the second power supply terminal;

a thirteenth transistor having a drain coupled to the first threshold node, a gate coupled to the second node, and a source coupled to the second power supply terminal;

a fourteenth transistor having a gate and a drain coupled to the drain of the twelfth transistor, and a source coupled to the first power supply terminal; and

a fifteenth transistor having a drain coupled to the second threshold node, a gate coupled to the gate of the fourteenth transistor, and a source coupled to the first power supply terminal.

5. The signal detection circuit of claim **4,** wherein the first, second, third, and fourth dual-gate transistors each further comprise:

a first transistor having a drain, a gate coupled to the first gate, and a source coupled to the first power supply terminal; and

a second transistor having a drain coupled to the second node, a gate coupled to the second gate, and a source coupled to the drain of the first transistor.

6. The signal detection circuit of claim **2**, further comprising a second comparator having an inverting input terminal coupled to a threshold terminal, a non-inverting input terminal coupled to the first output terminal, and an output terminal coupled to a second output terminal.

7. The signal detection circuit of claim **6**, wherein the second comparator further comprises:

a sixteenth transistor having a drain, a gate coupled to the first node, and a source coupled to the second power supply terminal;

a seventeenth transistor having a gate, a drain coupled to the first output terminal, and a source coupled to the drain of the sixteenth transistor;

an eighteenth transistor having a drain coupled to the threshold terminal, a gate coupled to the first output terminal, and a source coupled to the second power supply terminal;

a nineteenth transistor having a drain coupled to the threshold terminal, a gate coupled to the common node, and a source coupled to the first power supply terminal;

a differential to single-ended amplifier having a non-inverting input terminal coupled to the first output terminal, an inverting input terminal coupled to the threshold terminal, and an output terminal coupled to the second output terminal;

a logic inverter having an input terminal coupled to the second output terminal and an output terminal coupled to the gate of the seventeenth transistor.

8. The signal detection circuit of claim **4**, wherein the differential to single-ended amplifier further comprises:

a first transistor having a drain, a source coupled to the first power supply terminal, and a gate coupled to the second power supply terminal;

a second transistor having a drain, a source coupled to the drain of the first transistor, and a gate coupled to the differential to single-ended amplifier inverting input terminal;

a third transistor having a drain, a source coupled to the drain of the first transistor, and a gate coupled to the differential to single-ended amplifier non-inverting input terminal;

a fourth transistor having a gate and a drain coupled to the drain of the second transistor, and a source coupled to the second power supply terminal;

a fifth transistor having a gate and a drain coupled to the drain of the third transistor, and a source coupled to the second power supply terminal;

a sixth transistor having a drain, a gate coupled to the gate of the fourth transistor, and a source coupled to the second power supply terminal;

a seventh transistor having a gate and a drain coupled to the drain of the sixth transistor, and a source coupled to the first power supply terminal;

an eighth transistor having a drain coupled to the differential to single-ended amplifier output terminal, a source coupled to the first power supply terminal, and a gate coupled to gate of the seventh transistor; and

a ninth transistor having a drain coupled to the differential to single-ended amplifier output terminal, a source coupled to the second power supply terminal, and a gate coupled to the gate of the fifth transistor.

9. The signal detection circuit of claim **7**, wherein the logic inverter further comprises:

a first transistor having a drain coupled to the gate of the seventeenth transistor, a gate coupled to the second output terminal, and a source coupled to the first power supply terminal; and

a second transistor having a drain coupled to the gate of the seventeenth transistor, a gate coupled to the second output terminal, and a source coupled to the second power supply terminal.

10. The signal detection circuit of claim **7**, wherein the first and second input terminals are coupled to a differential input signal.

11. The signal detection circuit of claim **10**, wherein device sizes and a capacitive load of the first output terminal are selected such that a frequency response of said signal detection circuit is sufficiently slow that a change in polarity or transition of the differential input signal will not cause the signal at the second output terminal to change state.

12. The signal detection circuit of claim **11**, wherein the differential input signal has a differential amplitude.

13. The signal detection circuit of claim **12**, wherein the second output terminal will exhibit:

a high logic level when the differential input signal amplitude is less than a first comparator threshold voltage; and

a low logic level when the differential input signal amplitude is greater than a second comparator threshold voltage.

14. The signal detection circuit of claim **13**, wherein the first comparator threshold voltage is less than the second comparator threshold voltage.

15. The signal detection circuit of claim **14**, wherein the first and second thresholds are set in part by logic levels applied to the first, second, third, and fourth logic terminals.

16. A signal detection circuit for comparing an amplitude of a differential input signal to a threshold, said differential input signal including a true input signal and a complement input signal, said signal detection circuit comprising:

first and second matched input signal level-shifters;

a comparator threshold generation circuit; and

a two-stage comparator, wherein the first input signal level-shifter is coupled to the true input signal, and the second input level-shifter is coupled to the complement input signal, wherein the comparator threshold generation circuit is matched to the first and second matched input signal level-shifters and outputs first and second compare voltages, wherein a first stage of the two-stage comparator outputs a low signal if the more positive of the first and second level-shifted input signals is greater than the more positive of the first and second compare voltages, and wherein the second stage of the two-stage comparator amplifies the output of the first stage of the two-stage comparator.

17. The signal detection circuit of claim **16** wherein positive feedback is provided to inhibit comparator self-oscillation.

18. The signal detection circuit of claim **16** having a low bandwidth so as not output a momentary pulse presented at the differential input signal during a transition in the differential input signal.

19. A signal detection circuit which compares the amplitude of a differential input signal to a comparator threshold voltage, said signal detection circuit comprising:

a first and second matched input signal level-shifters, each having an output signal;

a compare voltage generation circuit; and

a two-stage comparator, wherein the differential input signal is comprised of a true input signal and a complement input signal, wherein the first input signal level-shifter is coupled to the true input signal and the second input level-shifter is coupled to the complement input signal, wherein the compare voltage generation circuit outputs a first compare voltage set to an average voltage of the output signals of the first and second matched level-shifters plus the comparator threshold voltage and a second compare voltage set to the average voltage of the output signals of the first and second matched level-shifters minus the comparator threshold voltage, wherein the first stage of the two-stage comparator outputs a low signal if the more positive of the first and second matched level-shifted input signals is greater than the more positive of the first and second compare voltages, and wherein the second stage of the two-stage comparator amplifies the output of the first stage of the two-stage comparator.

20. The signal detection circuit of claim **19** having positive feedback to inhibit comparator self-oscillation and a sufficiently low bandwidth so as not to pass to an output of the two stage comparator a momentary pulse presented at the differential input signal.